

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

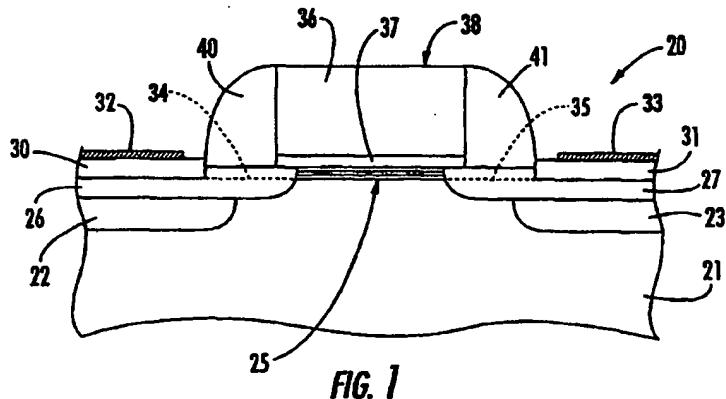
PATENT NO. : 6,833,294 B1
DATED : December 21, 2004
INVENTOR(S) : Mears et al.

Page 1 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Drawings.

Delete FIG. 1 and insert new FIG. 1



Column 1.

Line 43, delete "on a binary" insert -- on binary --

Line 67, delete "in a silicon" insert -- in silicon --

Column 2.

Line 1, delete "electromuminescence" insert -- electroluminescence --

Line 23, delete "Published-Great" insert -- Published Great --

Line 60, delete "superlattice and has" insert -- superlattice has --

Column 4.

Line 18, delete "tensor," insert -- tensor, --

Column 5.

Lines 11 and 60, delete "gate 35" insert -- gate 38 --

Column 7.

Line 63, delete "from the both" insert -- from both --

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 9,

Lines 44-46, delete "In other processes and devices the structures of the present invention may be formed on a portion of a wafer or across substantially all of a wafer."

Line 59, delete "also formed" insert -- also be formed --

Signed and Sealed this

Nineteenth Day of July, 2005



JON W. DUDAS
Director of the United States Patent and Trademark Office